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REMARKS

In response to the Office Action mailed July 3, 2002, Applicant respectfully requests reconsideration. To further the prosecution of this application, Applicant has amended the specification and submits the following remarks.

A. Telephone Conference with Examiner

Applicant's representative appreciates the courtesies extended by Examiner Nghiem in granting and conducting a telephone conference on September 30, 2002. During the conference, Applicant's representative and the Examiner discussed the priority date of the present application in view of the cited Cannata reference (U.S. Patent No. 5,811,808).

In particular, Applicant's representative explained to the Examiner that the parent case for the present divisional application was filed as a National Phase of PCT application No. PCT/US96/11014, which PCT application has a filing date of June 28, 1996. As set forth in MPEP §1893.03(b), the parent case accordingly has the filing date of the PCT application, namely, June 28, 1996. Pursuant to the priority claim in the present application under 35 U.S.C. §120, the present application therefore has the benefit of an effective filing date of June 28, 1996. Since the Cannata reference has a later filing date of September 12, 1996 and an issue date of September 22, 1998, it does not appear to qualify as prior art under any section of 35 U.S.C. §102.

After discussing the above situation, the Examiner indicated during the telephone conference that the Cannata reference seems to have been improperly asserted, and advised Applicant's representative to summarize the substance of the telephone conference in response to the Office Action.

In view of the foregoing, Applicant respectfully requests that the rejections of claims 1-5, 7, 9-13, 17, and 18 under 35 U.S.C. §102(b) as allegedly being anticipated by Cannata be withdrawn.

B. Amendments to the Specification

The specification has been amended to reflect the current status of the priority application (now issued as a patent) and to address various typographical and grammatical errors. In

particular, the specification has been amended to address inconsistencies in some reference characters for various features indicated in the drawings. For example, some references in the specification to particular features in one or more figures use different reference characters than those that appeared in the figures. The amendments herein address such inconsistencies but do not add any new matter to the disclosure.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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Attorney Docket No. L0501/7035
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x10/03/02

VERSION WITH MARKINGS TO SHOW CHANGES MADE

The paragraph beginning on page 1, after the title, has been amended as follows:

This application is a divisional of prior application No. 08/981,109, filed on May 26, 1998, entitled "DIGITAL OFFSET CORRECTOR" [and now PENDING], which is now U.S. Patent No. 6,274,869, issued August 14, 2001. This prior application No. 08/981,109 was filed as a National Phase of PCT application No. PCT/US96/11014, which PCT application was filed on June 28, 1996.

The paragraph beginning at page 6, line 26 has been amended as follows:

Figure 2 shows a schematic diagram of the array sensor of the invention. A microbolometer array 102 comprises the radiation sensing portion of the focal plane array 100. In one embodiment, the array 102 may comprise over 80,000 individual microbolometers. The electronic circuits associated with each microbolometer are shown in more detail in Figure 3. [The] A detector [ground] common 126 is distributed uniformly over the array 102. The array is arranged in a regular grid of microbolometers, by column line 114, addressed individually using a dynamic row select register 104 and column circuitry 110. The array 102 and the array's electronics may be tested during array production. The test clock 122, test data 124, test mode enable 116, global test enable 128 and detector test force 118 signals provide the control signals used to test the array. Column processing circuitry 200 is provided for each column line 114 in the array. The column processing circuity 110 is shown in more detail in Figure 5.

The paragraph beginning at page 7, line 5 has been amended as follows:

The array 102 has a distributed [ground] common 126 and a distributed global test enable 128. The array 102 is addressed using a dynamic row select register 104 and in a test mode a dynamic column select test register 108. In operation, column circuitry 200 addresses any particular column. Control 112 controls the operation of the column circuitry. The column circuitry can be disabled with disable line 119.

The paragraph beginning at page 7, line 10 has been amended as follows:

Figure 3 is a circuit schematic diagram of one portion of the microbolometer array of the invention showing an example of four detectors and associated detector electronics. The microbolometer array comprises a plurality of basic unit cells including multiplexer test transistors. In one embodiment the microbolometer focal plane array may comprise a 328 x 246 matrix of unit cells having 328 column circuits. The detector common [ground] 126 is connected to one side of bolometers 218A, 218B, 218C and 218D and unit cells 212A, 212B, 212C and 212D, respectively. The bolometers are connected in parallel with test transistors 220A, 220B, 220C and 220D. The "on" resistance of transistors 220A, 220B, 220C and 220D approximates that of the bolometers 218A, 218B, 218C and 218D. Thus, the test transistors can be used to provide a signal that emulates the bolometer signal. The emulated signal may be used to test the multiplexer circuitry before the bolometers are created. Such testing may result in less expensive manufacture because defective chips may be thus identified prior to final fabrication. Switches 222A, 222B, 222C and 222D switch the bolometer or test transistor signal in response to row select lines 216A and 216B. In a test mode the test transistors may be activated by the global test enable 128 and each individual row may be selected using one of the row select lines. An output is available at each column circuit 200A and 200B. In a test mode, the column circuitry 200A and 200B is bypassed and addressed with a column multiplexer.

The paragraph beginning at page 7, line 27 has been amended as follows:

Refer now to Figure 4 which shows one example of microbolometer array compensation circuitry of the invention. A bidirectional vertical shift register 104 functions as the row select for the array. Row select line 216 activates switch 222 to either select the signal from the bolometer 218 or the test transistor 220. A global test enable 128 activates all test transistors. The column line 114 is biased by a supply 117. The column line 114 is sensed by a buffered direct injection (BDI) circuit [132] 1704 having a preamplifier stage and an output transistor stage. The integration capacitor 180 integrates the signal on the column sense line 181. In one embodiment of the invention the integration capacitor may have an integration time of about 29 microseconds. An offset capacitor circuit 16 provides an initial offset signal 763 in order for the integration capacitor 180 to provide a more precise sample of the bolometer 218 signal. In one

embodiment, the offset capacitor 16 may be about 5 pF, and the integration capacitor may be about 10 pF. Comparator 20 compares the analog ramp 18 to the integrated signal on column sense line 181.

The paragraph beginning at page 8, line 7 has been amended as follows:

The ramp generator 134, shown in more detail below, provides the comparator with an analog ramp signal 18. The ramp signal, in one example, may be a 34 s r amp that may nominally range between about 5 volts to 10 volts. The comparator 20 provides a binary signal 21 to three elements: the offset capacitor circuit 16, analog-to-digital latches 150 and an overflow counter 138. In this embodiment, the digital offset corrector of the invention has two analog-to-digital conversion phases. A first phase is the "coarse" conversion phase and a second phase is the accurate conversion phase or "fine" conversion phase. The two phases provide an integrated analog-to-digital conversion by taking advantage of the architecture of the column circuitry. During the coarse conversion phase the ramp signal is held to its low value, about 4 volts in one example. The circuitry integrates and dumps the integration capacitor 180 a number of times. The number of times that the circuitry dumps the signal from the integration capacitor 180 depends upon the size of the integration capacitor and the background detector bias. The detector bias charge is usually much greater than the integration capacitor capability. As a result, the integration capacitor would be swamped by the bias signal. To avoid this, the capacitor integrates and resets a number of times. The capacitor 180 is reset to allow the bolometer signal to be integrated in a "fine" mode. The signal remaining on the capacitor will be representative of the voltage from the bolometer. The overflow counter 138 counts the number of times the capacitor is dumped. In the "fine" mode, a digital ramp signal 151 is provided from a 13 bit gray code counter encoder 146. The 13 bit gray code clock may operate using a frequency equal to 12 times the pixel clock, using four phases of the 12x_clock for 13 bit resolution. The digital ramp signal and the analog ramp signal are coordinated so that they start and end at the same time. Horizontal shift register 106 provides the offset sample and hold 142 with the proper column select signal [offset] 162 to set the offset capacitor 16. A digital offset [145] 353 is provided to a four bit digital-to-analog converter 144 and the offset input sample and hold 142 receives the analog output 301 of the four bit digital-to-analog converter 144. The digital offset 353 may be

advantageously latched with the pixel clock. The column [line 114] select signal 162 provides the addressing for the offset sample and hold 142 and the output latches and drivers 140. Depending on the column selected, the output latches and drivers provide the count of the overflow counter 138 and the count of the analog-to-digital converter latches 150, enabled by comparator 20. The output drivers 148 provide digital data 495 to the off focal plane circuits. The digital data 495 is a concatenation of the overflow counter and the analog-to-digital converter latches and may be clocked with the pixel clock. The analog ramp and digital ramp are started at the start of the "fine" mode phase.

The paragraph beginning at page 9, line 7 has been amended as follows:

Refer now to Figure 4A which shows an alternate example of microbolometer array compensation circuitry of the invention employing a bolometer offset compensator 701 connected in parallel with the detector elements. The compensation circuitry may advantageously be integrated onto a single integrated circuit with the focal plane array using, for example, MOS technology. It will be understood that the bolometer offset compensator and its control circuits are replicated for each column of detectors in the array. The alternate embodiment shown in Figure 4A optionally includes a nonlinear compensating voltage supply 703 coupled to load resistor 115. The load resistor 115 is connected to the bolometer offset compensator 701 and the column line 114. One embodiment of the bolometer offset compensator 701 is described in more detail below with reference to Figure 15. The bolometer offset compensator 701 is coupled at a first terminal to load resistor 115 and at a control input to data latch 744. The data latch 744 is described in more detail below with reference to Figure [21] 16. Digital offset data [745] 353 is provided to the data latch 744. The digital offset data represents the offset signal 761 to be applied to each row and column bolometer signal on column line 114. A BDI preamplifier 1704 amplifies the offset bolometer signal for further processing.

The paragraph beginning at page 10, line 3 has been amended as follows:

Referring now to Figure 5 which shows [an] a more detailed example of a circuit schematic diagram of the column circuit of the invention shown in Figure 4. Each column in the

array may be coupled to an associated column circuit as shown in Figure 5. The column circuit is centered around the comparator 20 which compares the voltage on the integration capacitor 180 with the reference voltage 18. The integration capacitor 180 is adjusted with an offset voltage 763 which is provided through transistor 176. The transistor has a bias signal which is controlled from off-chip electronics by a first bias signal and a second bias signal. The circuit has a charge injection capacitor 177. Bias 2 signal is provided through transistor 174 to set a bias voltage on the integration capacitor. Transistors 174, 176, and capacitor 177 form part of offset capacitor circuit 16. The coarse offset is provided by a sample and hold circuit 142 which is coordinated with the column select 162. An analog offset signal 301 is provided [on the offset bus 156] to the sample and hold circuit 142 from the four bit digital-to-analog converter 144 of Figure 4. Switch 158 may be selected by the column select 162 to provide the offset [voltage to] signal 301 a supply transistor 164. Alternately, if the offset [voltage 156] signal 301 is not supplied, a reference voltage VCS is provided through source 160 to transistor 166. The offset signal 171 is provided through switch 170 which is controlled by end of line transfer signal 172. Either the offset voltage is provided or a coarse/fine control voltage 21 is provided [from] via NAND gate 154. If the coarse/fine control 175 is active and the comparator is active, then the output of the NAND gate is inverted to supply a predefined constant offset voltage in response to switch 170 through the end of line transfer signal 172. The capacitor 180 integrates the signal from the bolometer which is preamplified by the BDI amplifier 1704. The column [bus signal 194 is provided by] line 114 provides a selected bolometer signal which is selected by the row select signal. The signal is biased by a global bias offset voltage of less than 20 volts through a 50K resistor 115, for example. The input signal may be disabled with transistor 190 in response to input disable signal 192 which is provided to eliminate the bolometer signal during certain phases of operation of the circuit. A transistor 186 amplifies the bolometer signal to the pass transistor 184. The transistor 186 is provided with a voltage from transistor 182 and is controlled by transistor 188. The pass transistor 184 allows the bolometer signal to be integrated on the integration capacitor 180. Integration capacitor 180 may be reset by switch 178 in response to reset signal 179. The output of the comparator 20 may be provided, in one example, to two sets of dynamic latches which allow the integration of column signals in a pipeline fashion where one signal is transmitted to the dynamic latch [196] 150 while the previous sample is being read out

of dynamic latch [198] 140. The gray code count signal [62, transfer reset signal 195, and a dynamic] 151 and the column select 162 from the horizontal shift register [108 signal is provided to] 106 are provided to the latches 150 and 140, and a bus switch [202 where the bus] 148 outputs the digital value 495 of the bolometer which has undergone coarse and fine conversion.

The paragraph beginning at page 11, line 3 has been amended as follows:

Refer now to Figure 6 which shows a digital-to-analog converter 144 as employed in one embodiment of the invention to provide the coarse offset signal to the integration capacitor. The offset signal on signal line 353 from the coarse offset controller 354 (Figure 7), B1, B2, B3 and B4, are provided to data flip-flops 251, 253, 255 and 257 respectively. The outputs of the flip-flops are sent to level shifters to adjust the voltage output to provide for the analog conversion. Level shifter 271 provides amplifier 281 with a voltage. Amplifier 281 controls transistor pair 291 to provide voltage to output 299. Level shifter 273 controls operational amplifier 283 to control the gate of transistor pair 293. Level shifter 275 provides the voltage to amplifier 285 which controls the gate of transistor pair 295. Level shifter 277 controls amplifier 287 which controls the gate of transistor pair 297. Transistor pairs 291, 293, 295, 297 are all connected to output 299 which is provided to operational amplifier 298 which provides the analog signal 301 representing the four bit digital number.

The paragraph beginning at page 12, line 16 has been amended as follows:

Now referring to Figure 8 which shows a more detailed circuit schematic of a fine offset controller 352 as employed in one embodiment of the invention. The fine offset controller may comprise a clipping controller 373, a scaler 372, a first fine offset multiplexer 357 and a second fine offset multiplexer 363. The fine offset memory 358 may have a 16-bit interface to an output 305 of a first fine offset multiplexer 357. In one embodiment, the first fine offset multiplexer 357 accepts write data on line 301 from an external data source or from the output of a new fine summation node 361. The coarse offset adjust signal 359 is provided to the new fine summation node 361 by the coarse offset controller 354 shown in Figure 7. The output of summation node 361 is multiplexed by the first fine offset multiplexer 357 with the external data 301 to provide[s] data 305 for the fine offset memory 358. The fine offset memory 358 contains fine offset

information for particular pixel elements in the FPA 100. The output of the fine offset memory 358 is multiplexed with an offset base 307 which provides a mechanism to bypass the offset in response to the offset bypass signal 309.

The paragraph beginning at page 19, line 32 has been amended as follows:

Now refer to Figure 15 which shows an alternate embodiment of a bolometer offset compensator circuit as contemplated by the present invention. As described above each column of the focal plane array is coupled to a bolometer offset compensator 701. Thus the bolometer offset compensator 701 and associated circuits, designated by arrow 707, are replicated on the FPA integrated circuit chip for each of the M columns. The bolometer signal on column line 114 is selected with row select line 216 to connect to BDI preamplifier 1704. The signal from the bolometer on column line 114 is the signal being compensated by the bolometer offset compensator 701. In the example shown, the bolometer offset compensator 701 comprises first through sixth compensating resistors, some of which are shown for illustrative purposes as compensating resistors 702, 704, and 708, each individually coupled to a plurality of switches 710A, 710B and 710D. The plurality of switches are coupled and controlled by the outputs 711A, 711B, and 711D of, for example, a six bit data latch 744. The six bit data latch 744 is enabled by the horizontal shift register 106. Digital offset data [745] 353 selects the particular resistor combination through data latch 744. In one embodiment of the invention, the first through sixth compensating resistors may have values in the nominal range of 1200 ohms to 8200 ohms and are coupled to a load resistor 115 of about 145 kohms, for example. The embodiments shown herein are meant by way of illustration, not limitation, and other equivalent values and combinations of compensating resistances or equivalent circuitry may be used without departing from the spirit and scope of the invention. In one embodiment (Figure 4A) nonlinear compensating voltage supply 703 supplies voltage 762 to the bolometer offset compensator 701.

The paragraph beginning at page 21, line 23 has been amended as follows:

Having described the elements of the bolometer offset compensator circuitry it will be helpful to the understanding of the invention to now describe the operation of the bolometer

offset compensator circuitry. By way of further background, microbolometer focal plane arrays typically require electronic circuits with a very large dynamic range in order to simultaneously accommodate both detector nonuniformities and very low signal levels. A dynamic range in excess of 1 million to 1 is typical. Electronic circuit switches can meet this difficult requirement, especially when applicable to large focal plane arrays, and provide a significant benefit and a practical application of microbolometer technology. In the embodiment shown in Figure 15, the nonlinear compensating voltage supply 703, when employed, may [preferably] be an off-focal plane nonlinear compensating voltage supply connected to on-focal plane circuits comprising the bolometer detectors 218, load resistor 115, [pre-amplifier] preamplifier 1704 and compensating resistors 702, 704, and 708. When a voltage, [V1] 762, is applied, a current flows through the detector column line 114, load resistor 115 and at least one compensating resistor as selected by opening one or more of the plurality of switches 710A - 710D. In some embodiments, load resistor 115 may not be required. [Voltage] A voltage at node V1 is set by a BDI preamplifier 1704 and is nominally the same voltage for each of M detector circuits. The current which flows into the preamplifier 1704 represents the signal current. To compensate for differences in detector resistance where the detector resistance may vary significantly from detector to detector the compensating resistors may be employed. If such compensating resistors are not employed, the preamplifier circuit must have a significantly increased dynamic range in order to accommodate not only the useful signal current, but also significant additional current resulting from detector resistance variations.

The paragraph beginning at page 22, line 11 has been amended as follows:

As current is applied to the bolometer detectors, I^2R heating raises the temperature of each detector. The increased temperature results in a change in detector resistance, thereby increasing the input dynamic range requirement of the BDI preamplifier 1704. The external nonlinear compensating voltage supply [117] 703 senses the current change at node V1, and provides a nonlinear voltage precisely compensating for I^2R heating induced changes in preamplifier current. In this way, the nonlinear voltage also reduces the dynamic range requirement of the preamplifier [circuit] 1704 to a level that may be readily achieved in an electronic circuit integrated onto the focal plane.

The paragraph beginning at page 22, line 18 has been amended as follows:

Reference is now made to FIG. 17 which is an overall schematic block diagram of the analog-to-digital converter of the invention. Analog input signal [15,] 181 the analog signal to be converted, is connected to one input of an unclocked analog comparator 20. The other input of the comparator 20 is connected to an analog ramp signal 18. Analog waveform generator [30] 134 generates the analog ramp signal 18. When the analog ramp signal 18 substantially equals the analog input signal [15,] 181 the comparator generates output signal 21. The comparator output signal 21 is connected to a control input of a metastability resolving circuit 35. Synchronized with the analog waveform generator [30] 134 is a Gray code generator [45] 146 that generates a digital Gray code 151 on a digital Gray code bus 62. The digital Gray code bus 62 is connected to a data input of the metastability resolving circuit 35. The metastability resolving circuit 35 stores the states of the digital Gray code 151 on bus 62 in response to an active state of the comparator output signal 21. As a result, the digital output signal 47 of the metastability resolving circuit 35 is a digital representation of the magnitude of the analog input signal [15] 181 when the magnitude of the analog ramp signal 18 equals the magnitude of the analog input signal [15] 181.

The paragraph beginning at page 22, line 32 has been amended as follows:

Reference is now made to FIG. 18, which illustrates the metastability resolving circuit 35 in more detail. Comparator output signal 21 is connected to the control input of an N-Bit data latch 11. N is the number of bits of resolution that the analog signal [15] 181 is digitized (converted) into by the analog-to-digital converter. N can be any number and is typically between eight and sixteen for most applications. The N-bit data latch 11 data input is connected to the digital Gray code bus 62 from the Gray code generator [45] 146. The data latched by the N-bit data latch 11 (which is a code generated by Gray code generator [45] 146) is provided on line 17 to N-bit flip-flop 19. N-bit flip-flop 19 resolves the metastability of the system by storing the data on line 17 a predetermined time period after the N-bit data latch 11 has stored the state of the Gray code generator [45] 146. The digital output 47 is provided as described above.

The paragraph beginning at page 23, line 10 has been amended as follows:

Reference is now made to FIG. 18A, which illustrates a schematic block diagram of analog waveform generator [30] 134 illustrated in FIG. 17. Operational amplifier 32 provides the analog ramp signal 18 by providing an output signal to integration capacitor 28. RESET signal 34 is generated by timing circuit 33 and activates switch 28A to discharge capacitor 28 when a new conversion is to be initiated. One input 39 of operational amplifier 32 in connected to a RAMP_BIAS signal and a second input 23 in connected to the output of a programmable current source 31. Programmable current source 31 is controlled by operational transconductance amplifier 27. Amplifier 27 has a first input connected to the analog ramp signal 18. A second input of amplifier 27 is connected to a ramp reference voltage RAMP_REF. A third input of amplifier 27 is connected to the output of ramp adjust circuit 29. The starting voltage of the analog ramp is adjustable by changing the RAMP_BIAS voltage. The slope of the analog ramp signal 18 is controlled by amplifier 27. By changing the output of programmable current source 31 in response to a current signal 27A from transconductance amplifier 27, the slope of the analog ramp signal 18 can be changed. In response to control signal 33A from timing circuit 33, issued just before ramp signal 18 is to terminate, ramp adjust circuit 29, via control signal 29A, turns amplifier 27 on to sample the difference between the RAMP_REF voltage and the voltage of analog ramp signal 18. Transconductance amplifier 27 converts this voltage difference to a current 27A that is used to control programmable current source 31. After programmable current source 31 has been adjusted, timing circuit 33, via control signal 33A, turns amplifier 27 off to open the feedback loop, issues RESET signal 19 to discharge capacitor 28 using switch 28A, and then opens switch 28A to begin another integration cycle.

The paragraph beginning at page 23, line 30 has been amended as follows:

Reference is now made to FIG. 19, which is a schematic block diagram of parallel analog-to-digital converters 10A and 10B. Only two converters are shown for clarity; there could be m number of converters in an array. In one preferred embodiment there are 328 converters in an array. Each analog-to-digital converter is connected to the digital Gray code bus 62 and an output bus 57. The digital Gray code bus 62 is connected to each data input of the m data latches. For clarity, only the connections to data latches 24A and 24B are shown. The data

input of each data latch is driven by the gray code generator [45] 146. The N-bit output bus 57 is connected to the data output of each transfer latch (latches 26A and 26B being illustrated) and is read by multiplexer readout circuit 59.

The paragraph beginning at page 24, line 6 has been amended as follows:

The analog signal on line [15A] 181A, the signal to be converted, is stored by capacitor [23A] 180A until sampling switch 12A is closed, thereby transferring the charge to capacitor 16A. Capacitor 16A integrates the analog signal [15A] 181A until switch 12A is opened. After a predetermined time interval has passed, switch 12A is opened and switch [23A] 25A is closed, thus resetting capacitor [23A] 180A at the start of each conversion period. Those skilled in the art will recognize that any charge transfer device or circuit may be used to transfer the signal to be compared. During the read out phase the sampled signal 14A is compared to an analog ramp signal 18 by comparator 20A. When the sampled signal 14A is equal to or at some predetermined potential with respect to the analog ramp signal 18, the output 22A of the comparator 20A activates latch 24A. The output of the comparator 20A is connected to the enable input of latch 24A. The latch 24A, connected to digital Gray code bus 62, stores the state of the gray code count at the time the analog ramp signal 18 equals the sampled signal 14A in response to comparator output signal 22A. The output of latch 24A is provided to a transfer latch 26A. Output control shift register 54, connected to transfer latches 26A and 26B, selects the output of a particular analog-to-digital converter from the array of converters. The output of each transfer latch is connected to sense amplifier 53 via N-bit output bus 57, part of multiplexer readout circuit 59. Only one transfer latch is active and supplying an output to bus 57 at any one time. The output control register 54 is synchronized with input clock 68.

The paragraph beginning at page 25, line 15 has been amended as follows:

Gray code generator [45] 146 will now be described. The digital Gray code 151 on bus 62, which in one embodiment of the invention is an N-bit binary gray code, is generated by concatenation of three bit streams: a least significant bit 60, a next-to-least significant bit 58 and a N-2 bit gray code word 56. The high speed clock 64 clocks an N-2 bit synchronous binary counter 48. The N-2 bit synchronous counter 48 provides an output signal to an N-2 bit Gray

code encoder 46. The Gray code encoder provides the N-2 most significant bits 56 of the digital Gray code on bus 62. Gray code encoder 46 provides a Gray code by XORing each bit output by counter 48 with an adjacent output bit.